AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): An apparatus for selectively converting a clock frequency in a digital signal receiver, comprising:

a first phase locked loop that outputs a first clock frequency;

a second phase locked loop that outputs a second clock frequency;

a switching portion for selecting ~~a~~either the first clock frequency from ~~one of~~ the first phase locked loop ~~and~~ or the second clock frequency from the second phase locked loops according to a predetermined control signal;

a format converter for receiving either of a first input digital signal and a second input digital signal, according to which of the first and second input digital signals is present, the format converter for converting the input digital signal received by the format converter into a predetermined display format output signal; and

a controller for controlling the switching portion to select and output the clock frequency corresponding to a frame rate of the input digital signal.

2. (currently amended): The apparatus of claim 1, wherein the first phase locked loop generates a clock frequency of 74.25 MHz, and wherein the second phase locked loop generates a clock frequency of ~~74.175~~ 74.176 MHz.

3. (currently amended): An apparatus for selectively converting a clock frequency in a digital signal receiver, comprising:

a first phase locked loop;

a second phase locked loop;

a switching portion for selecting a clock frequency from one of the first and second phase locked loops according to a predetermined control signal;

a format converter for receiving either of a first input digital signal and a second input digital signal, according to which of the first and second input digital signals is present, the format converter for converting the input digital signal received by the format converter into a predetermined display format output signal; and

a controller for controlling the switching portion to select and output the clock frequency corresponding to a frame rate of the input digital signal,

~~The apparatus of claim 1,~~ wherein the input digital signal has a frame rate selected from the group consisting of 60 Hz, 59.94 Hz, 30 Hz, 29.97 Hz, 24 Hz and 23.97 Hz, wherein if the frame rate of the input digital signal is one of 60 Hz, 30Hz and 24 Hz, the controller controls the switching portion to select and output the clock frequency of the first phase locked loop, and wherein if the frame rate of the input digital signal is one of 59.94 Hz, 29.97 Hz and 23.97 Hz, the controller controls the switching portion to select the clock frequency from the second phase locked loop.

4. (currently amended): The apparatus according to claim 3 wherein the clock frequency of the first phase locked loop is 74.25 MHz, and wherein the clock frequency of the second phase locked loop is ~~74.175~~ 74.176 MHz.

5. (canceled).

6. (previously presented): A digital signal receiver comprising:

a video decoder for decoding a video component of a received digital signal into a first input digital signal;

an analog to digital converter for converting a received analog video signal into a second input digital signal;

a format converter for receiving either of said first and second input digital signals, according to which of said first and second input digital signals is present, said format converter for converting the input digital signal received by said format converter into a predetermined display format output signal;

a controller for detecting a frame rate of the input digital signal received by said format converter and outputting a timing control signal corresponding to the frame rate detected; and

clock frequency providing means for providing a clock frequency according to the timing control signal output by said controller, said clock frequency provided to the format converter for converting the input digital signal received by said format converter into said predetermined display output signal; said clock frequency also provided to said video decoder when said second input digital signal is not present at said format converter;

wherein said clock frequency providing means comprises:

a first phase locked loop for generating a first clock frequency;

a second phase locked loop for generating a second clock frequency; and

a switching portion that receives said timing control signal from said controller and said switching portion outputting one of said first and second clock frequencies corresponding to the received timing control signal as said clock frequency.

7. (original): The digital signal receiver according to claim 6, further comprising an on-screen graphics mixer for mixing desired graphics with said predetermined display format output signal to output a mixed graphics video signal, wherein said on-screen graphics mixer operates responsive to the clock frequency provided by said clock frequency providing means.

8. (original): The digital signal receiver according to claim 7, further comprising a video signal processor for processing the mixed graphics video signal output from said on-screen graphics mixer.

9. (original): The digital signal receiver according to claim 7, further comprising audio signal processing means for processing audio signals received in said digital signal receiver.

10. (canceled).

11. (previously presented): A method of adapting clock frequency in digital signal receiver to correspond with a frame rate of an input broadcast signal, said method comprising:

receiving said input broadcast signal into said digital signal receiver;

detecting a frame rate of the input broadcast signal received;

selecting a clock frequency that corresponds to the frame rate which is detected; and

outputting the clock frequency which is selected to components of the digital signal receiver that use the clock frequency to convert the input broadcast signal into a predetermined display format output signal;

wherein the step of selecting the clock frequency comprises, outputting a control signal from a controller, said control signal depending upon the frame rate which is detected; receiving said control signal into a selector, said selector connected to outputs of a plurality of phase locked loops, wherein each phase locked loop has a predetermined clock frequency, and selecting one predetermined clock frequency of one of said plurality of phase locked loops based upon the control signal received by the selector.